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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	Art Unit: 2822
Shunpei YAMAZAKI et al.	)	Examiner: M. Wilczewski
Serial No. 08/691,434	)	
Filed: August 2, 1996	)	
For: METHOD OF FABRICATING	)	
SEMICONDUCTOR DEVICES AND	)	
APPARATUS FOR PROCESSING A	)	
SEMICONDUCTOR	)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, the Applicants submit herewith a Form PTO-1449 listing references known to the Applicants and request that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Japanese Patent Office cited JP 04-063414, JP 05-021382 and JP 05-259259 in a rejection dated April 21, 2004, against an application which is a Japanese counterpart of the present application. U.S. Patent Nos. 5,344,522 and 5,490,896, both to Yagi et al., are in the family of JP 04-063414.

The rejection dated April 21, 2004, asserts that Figure 1 of JP 04-063414 shows a "latent image chamber 6" which corresponds to "a chamber for irradiating a laser light" of the Japanese counterpart of the present application and that it is a known technology to load and unload a substrate to be treated by using a cassette.

The rejection dated April 21, 2004, further asserts that Figure 4 of JP 05-259259 shows a preliminary treatment chamber 4A which corresponds to "a third treatment

chamber for heating a substrate" of the Japanese counterpart of the present application and that it is a known technology to load and unload a substrate to be treated by using a cassette.

The Japanese Patent Office cited JP 63-318125, JP 03-201538, JP 04-221854, JP 04-278925, JP 04-286367, JP 04-286370 and the Nikkei Microdevices article in two rejections dated April 27, 2004, against an application which is a Japanese counterpart of the present application. U.S. Patent No. 5,534,884 to Mase et al. is in the family of JP 04-278925.

The first rejection dated April 27, 2004, asserts that there are two differences between the invention as claimed in claim 1 of the Japanese counterpart of the present application and the invention described in JP 63-318125 (in particular, page 3, line 4 of the upper-left-hand column to page 4, line 13 of the upper-right-hand column). First, in the invention as claimed in claim 1 of the Japanese counterpart of the present application, a semiconductor treatment apparatus comprising a doping first chamber, an etching second chamber and a third chamber for irradiating a laser light is used to transport a substrate to be treated among the respective chambers without exposing the substrate to outside air. On the contrary, JP 63-318125 does not describe transporting such a substrate among respective chambers without exposing the substrate to outside air. Second, in the invention as claimed in claim 1 of the Japanese counterpart of the present application, a laser light is irradiated after etching an insulating film. On the contrary, JP 63-318125 describes a lamp annealing conducted after etching an insulating film.

not method claims

The first rejection dated April 27, 2004, further asserts, with respect to the first difference, that before filing the Japanese counterpart of the present application it is a known technology to form a semiconductor device by using a multi chamber so that an etching step and thermal treatment steps such as film formation and crystallization, and activation of an impurity are conducted continuously without exposure to outside air in order to improve throughput and to prevent a substrate to be treated from being polluted, as it is described, for example, in the Nikkei Microdevices article (in particular, pages 34-39) and in JP 04-251921 (cited in the Information Disclosure Statement filed August 10, 1998, in particular, paragraphs 1-44). The rejection asserts that a skilled

person is capable of conducting an impurity doping and an etching of an insulating film, and an activation of an impurity described in JP 63-318125 by using a multi chamber.

The first rejection dated April 27, 2004, further asserts, with respect to the second difference, that before filing the Japanese counterpart of the present application, it is merely a known technology to activate an impurity by a laser light, as it is described in JP 04-221854 (in particular, see paragraph 38) and in JP 03-201538 (in particular, see page 3, line 4 of the lower-left-hand column to page 3, line 16 of the lower-left-hand column).

The first rejection dated April 27, 2004, further asserts the following differences between the invention as claimed in claims 2 and 4 of the Japanese counterpart of the present application and the invention described in JP 63-318125. In the invention as claimed in claims 2 and 4 of the Japanese counterpart of the present application, a semiconductor film is formed over a substrate, and is patterned to provide an active layer. On the contrary, in the invention described in JP 63-318125, a semiconductor substrate is used as an activation layer. However, it is a known technology before filing the Japanese counterpart of the present application to form a semiconductor device with a TFT using a patterned semiconductor film as an active layer over a substrate.

The first rejection dated April 27, 2004, further asserts, with respect to claim 3 of the Japanese counterpart of the present application, that a region of a handling system described in Figure 2 of the Nikkei Microdevices article corresponds to a preliminary chamber claimed in claim 3 of the Japanese counterpart of the present application.

The first rejection dated April 27, 2004, further asserts, with respect to claim 5 of the Japanese counterpart of the present application, that it is merely a known technology before filing the Japanese counterpart of the present application to activate an impurity by an excimer laser light, as it is described, for example, in JP 04-221854 (see, in particular, paragraph 38), and in JP 03-201538 (see in particular page 3, line 4 of the lower-left-hand column to page 3, line 16 of the lower-left-hand column).

The first rejection dated April 27, 2004, further asserts, with respect to claim 6 of the Japanese counterpart of the present application, that it is merely a known technology before filing the Japanese counterpart of the present application to dope an impurity by a plasma doping, as it is described, for example, in JP 03-201538 (see in

particular page 3, line 4 of the lower-left-hand column to page 3, line 16 of the lower-left-hand column).

The first rejection dated April 27, 2004, further asserts, with respect to claim 9 of the Japanese counterpart of the present application, that it is a known technology before filing the Japanese counterpart of the present application to use an ion containing phosphorus as an impurity ion to be doped.

The second rejection dated April 27, 2004, further notes a description in paragraphs 7-30 of JP 04-286370 and that it is considered that a plasma doping step and a rapid thermal annealing step are generally conducted in separate chambers (reaction chambers).

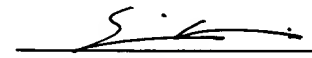
The second rejection dated April 27, 2004, further asserts that claim 7 of the Japanese counterpart of the present application has been compared with the invention described in JP 04-286370 (see in particular paragraphs 7-30). In the invention as claimed in claim 7 of the Japanese counterpart of the present invention, the semiconductor device has a CMOS structure. On the contrary, the invention described in JP 04-286370 does not have a CMOS structure.

The second rejection dated April 27, 2004, further asserts that it is merely a known technology to form a semiconductor device in a CMOS structure by forming first and second semiconductor films over a substrate, and forming a first gate electrode over the first semiconductor film through a first gate insulating film, and forming a second gate electrode over the second semiconductor film through a second gate insulating film, and implanting a boron ion into the first semiconductor film using the first gate electrode as a mask with the second semiconductor film covered with a resist mask, and removing the resist mask covering the second semiconductor film, and implanting an ion containing phosphorus into the first and second semiconductor films, and subsequently activating the ions implanted into the first and second semiconductor films, as it is described in JP 04-286367 (see in particular paragraphs 15-39) and in JP 04-278925 (see paragraphs 28-38).

This Information Disclosure Statement is being submitted with an RCE. Therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280. A duplicate copy of this sheet is attached.

Respectfully submitted,



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